Analysis and Applications of Parasitic Capacitance Cancellation Techniques for EMI Suppression

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***Abstract*—This paper reviews and analyzes five parasitic capacitance cancellation methods. Critical parameters and constraints determining the cancellation frequency ranges are identified, and the effective frequency range for each cancellation method is derived based on these constraints. Due to these constraints, each method has specific advantages for certain applications. The cancellation techniques, which all make use of either mutual capacitance or mutual inductance, are applied to different applications based on their advantages, and the experiments are carried out to verify the analysis.**

***Index Terms*—Common-mode (CM) noise, mutual capacitance, mutual inductance, parasitic capacitance, parasitic capacitance cancellation.**

I. Introduction

THE PARASITIC capacitance between high dv/dt nodes and the ground is a major contributor to common-mode (CM) electromagnetic interference (EMI) noise in a power electronics system. The CM current is generated from the charging and discharging of the parasitic capacitance between the high dv/dt nodes and the ground. The power devices in power electronics systems have switching and conduction power losses. The heat generated from power losses is conducted to the air via the heat sinks attached to the power devices. In order to reduce the thermal resistance between the power devices and the heat sinks, the power devices have a large attaching area and a very small distance to the heat sinks. Because of this, the parasitic capacitance between the heat sinks and the power devices is usually not small.

In some applications, the heat sinks are connected to the "hot" ground of the system so that most of the noise current can flow directly back to the circuits. For safety reasons, these heat sinks must be unreachable from outside. However, when the heat sinks are large, particularly for high-power applications, they are usually mounted on the grounded frames or the chassis of the systems. Thus, the CM noise current can easily go to the Earth ground. For many conventional power conversion topologies, such as buck, forward, boost, buck–boost, and flyback, the power switches are always connected to an inductor. If a negative capacitance can be generated with the help of the inductor, it would be possible to cancel the parasitic capacitance between the power devices and the heat sinks.

In addition to the parasitic capacitance discussed above, the parasitic capacitance within an inductor is also very important to EMI noise suppression. The inductor is a very important component for EMI suppression in power electronics systems. Due to the voltage gradients in inductor windings, there is always an electric field distributed between turns, between windings, and between windings and cores. The effects of the electric field can be represented with a lumped parasitic capacitance. An ideal inductor has an impedance that is proportional to the frequencies. In contrast, a practical inductor cannot achieve this at high frequencies (HFs) because of the effects of the parasitic capacitance. To effectively block EMI noise at HFs, the parasitic capacitance should be greatly reduced.

Several methods have been developed to cancel the effects of parasitic capacitance [1]–[6]. However, their performance at HFs and their applications in power electronics systems have not been carefully studied. Such a study would be very important since only after its HF behavior, constraints and applications are identified, can a method be effectively used to suppress EMI noise.

This paper studies the HF performance of these parasitic cancellation techniques. The critical parameters, frequencies, and methods to improve their HF performance are discussed as well. The applications of different parasitic cancellation techniques are also explored.

II. Parasitic Capacitance Cancellation Techniques

There are two ways of generating a negative capacitance to cancel parasitic capacitance. One is to use mutual capacitance theory, and the other is implemented with the help of mutual inductance. Both of these methods are discussed below, and their constraints are identified.

A. Parasitic Capacitance Cancellation Using Mutual Capacitance Concept

1) Principles: A four-conductor system is shown in Fig. 1. There are six capacitances between these four conductors. The mutual capacitance defined here is different from that defined in most literature. The mutual capacitance in most other literature is defined between two conductors, such as C_{12} in Fig. 1(b); however, the mutual capacitance as used here is defined between two capacitors. If conductors 1 and 2 are grouped as capacitor C_1 and conductors 3 and 4 are grouped as capacitor

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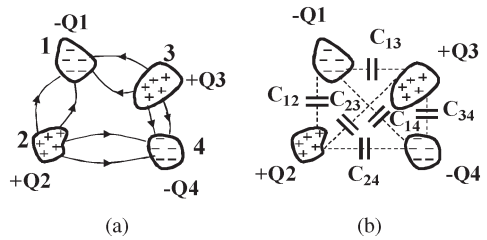

Fig. 1. Conventional definition of mutual capacitance. (a) Four conductors carrying different electric charges. (b) Capacitance within four conductors.

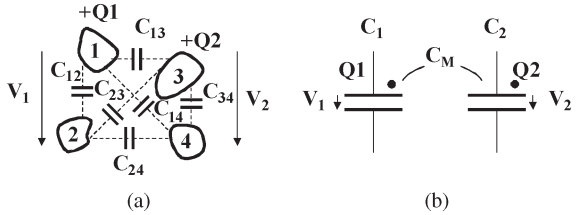

Fig. 2. Definition of mutual capacitance between two capacitors. (a) Grouping conductors as two capacitors. (b) Definition of mutual capacitance between two capacitors.

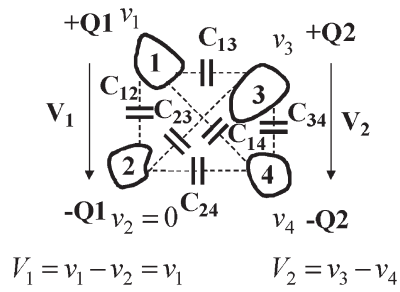

Fig. 3. Calculation of mutual capacitance between two capacitors.

C_2, the mutual capacitance $C_{\rm M}$ between these two capacitors can be defined as in Fig. 2.

In (1), the charge carried on C_1 is the result of voltage V_1 added to C_1 and voltage V_2 added to C_2. The mutual coupling effects of V_2 on C_1 are represented by mutual capacitance $C_{\rm M}$. Mutual capacitance occurs when two capacitors are close to each other and the electric fields are not fully confined within the capacitors. When this happens, the capacitors' electric fields launch to other conductors nearby; as a result, electric charges are induced on the nearby capacitors. In Fig. 2(b), capacitances C_1 and C_2 and the mutual capacitance $C_{\rm M}$ represent the effects of C_{12}, C_{13}, C_{14}, C_{23}, C_{24}, and C_{34}. If conductor 2 is selected as the voltage reference $v_2 = 0$, the voltage potentials of the other conductors are v_1, v_3, and v_4, as shown in Fig. 3.

Since the capacitance between two conductors has nothing to do with the electric charges that they carry, for convenience, it is assumed that conductors 1 and 2 (capacitor C_1) carry electric charge Q_1 and $-Q_1$, respectively; and conductors 3 and 4 (capacitor C_2) carry electric charge Q_2 and $-Q_2$, respectively. The relationship between the capacitance and the charges carried by each capacitor can be expressed as

$$\begin{aligned} Q_1 &= C_1 V_1 + C_M V_2 \\ Q_2 &= C_M V_1 + C_2 V_2. \end{aligned} \tag{1}$$

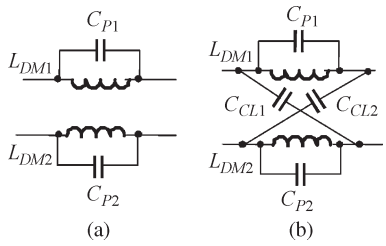

Fig. 4. Method 1: cancellation of winding capacitance with the mutual capacitance concept. (a) DM inductor with parasitic capacitance $C_{\rm P1}$ and $C_{\rm P2}$. (b) Cancellation of $C_{\rm P1}$ and $C_{\rm P2}$ (method 1).

Based on (1), the equivalent C_1, C_2, and $C_{\rm M}$ capacitances can be solved in (2). It is shown in (2) that $C_{\rm M}$ is a function of C_{13}, C_{14}, C_{23}, and C_{24}. These are the capacitances between capacitors C_1 and C_2. C_1 and C_2, on the other hand, are determined not only by the capacitance between the two conductors inside the capacitors, but also by the capacitance between the two capacitors, i.e.,

$$\begin{cases} C_1 = C_{12} + \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 = C_{34} + \frac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_M = \frac{C_{23}C_{14}-C_{13}C_{24}}{C_{13}+C_{14}+C_{23}+C_{24}}. \end{cases} \tag{2}$$

Equation (2) shows that the capacitor's self-capacitances C_1 and C_2 are always larger than capacitances C_{12} and C_{34} between two conductors inside the capacitors. The closer the two capacitors are, the larger C_{13}, C_{14}, C_{23}, and C_{24} will be, and therefore, the larger C_1 and C_2 become.

The condition for zero mutual capacitance $C_{\rm M}$ is

$$C_{23}C_{14} = C_{13}C_{24}. \tag{3}$$

To null the mutual couplings between two capacitors, the product of the capacitance on diagonal branches should be equal to the product of the capacitance on the top and bottom branches. The relationship described in (3) is also the balance condition for the Wheatstone bridge, which is composed of C_{13}, C_{14}, C_{23}, and C_{24}. Thus, the null condition (3) can also be explained using the Wheatstone bridge concept.

The condition for zero mutual capacitance can be used to cancel parasitic capacitance, such as the winding capacitance of a differential mode (DM) inductor, which is not desirable in many EMI noise reduction applications. This cancellation method is shown in Fig. 4 and is referred to as method 1. The DM inductor in Fig. 4(a) is a balanced structure with two identical inductors on each side. Due to the physical structure of the inductors, there is always a turn-to-turn and turn-to-core parasitic capacitance. The effect of this capacitance can be represented by equivalent parallel capacitances $C_{\rm P1}$ and $C_{\rm P2}$ on the two windings. The effects of $C_{\rm P1}$ and $C_{\rm P2}$ are detrimental to the HF impedance of the inductors and the ability of the inductor to block HF EMI noise. Therefore, $C_{\rm P1}$ and $C_{\rm P2}$ should be as small as possible. If $C_{\rm P1}$ and $C_{\rm P2}$ correspond to C_{13} and C_{24} in Fig. 3, the two small capacitors $C_{\rm CL1}$ and $C_{\rm CL2}$, which correspond to C_{14} and C_{23} in Fig. 3, are diagonally connected to cancel $C_{\rm P1}$ and $C_{\rm P2}$, as shown in Fig. 4(b).

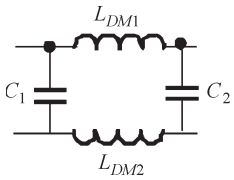

Fig. 5. Resultant π-type EMI filter.

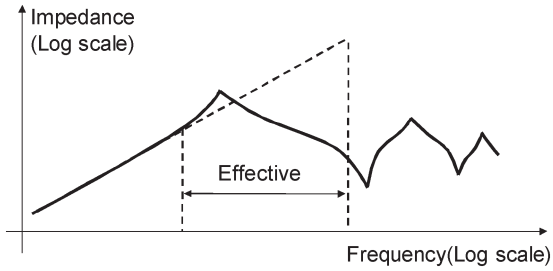

Fig. 6. Effectiveness of parasitic capacitance cancellation.

Applying the capacitors in Fig. 4(b) to Fig. 3, the corresponding values of C_{12} and C_{34} are zero. If the product of $C_{\mathrm{L}1}$ and $C_{\mathrm{L}2}$ is equal to the product of $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$, the effects of $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$ are canceled. Two shunt capacitors C_1 and C_2, whose values are given by (2), are generated on two sides. The resultant network is a π-type EMI filter, as shown in Fig. 5. In Fig. 5, the winding capacitance is not only canceled, it is also used as a filtering component in the EMI filter.

The first advantage of method 1 is that it does not have any requirements for the coupling of the inductor, and hence, the cancellation is not constrained by nonideal couplings, which are encountered in the other methods discussed later. The second advantage is that the cancellation capacitance does not need to be grounded, and therefore, no leakage current is generated to the ground.

2) Effectiveness of Cancellation: Fig. 4(b) shows that the two inductors and their parasitic winding capacitances $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$ are not necessarily equal. The cancellation capacitances $C_{\mathrm{CL}1}$ and $C_{\mathrm{CL}2}$ are also not necessarily equal. As long as the product of $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$ is equal to the product of $C_{\mathrm{CL}1}$ and $C_{\mathrm{CL}2}$, the effects of $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$ can be canceled. Thus, in a practical design, adjusting the value of only one cancellation capacitor can achieve cancellation.

The cancellation is based on the lumped parasitic capacitance model in Fig. 4(a). For the model in Fig. 4(a), $C_{\mathrm{P}1}$ and $C_{\mathrm{P}2}$ can only represent the first parallel resonance between the inductor and the parasitic capacitance. When the frequency of interest is very wide, there are more series and parallel resonances observed, as shown on the typical impedance curve in Fig. 6 [7], where both frequency and impedance are in logarithmic scale. The inductor can no longer be represented using the simple model in Fig. 4(a). Hence, the cancellation will work only for a parasitic capacitance with first-order approximation. For the second-order and higher order parasitics, it may not achieve cancellation. Another constraint is that this method should be used to cancel the parasitic capacitance of DM inductors only, since it requires inductors on both sides. In CM inductors, no inductor is on the ground side, so it is difficult to apply it.

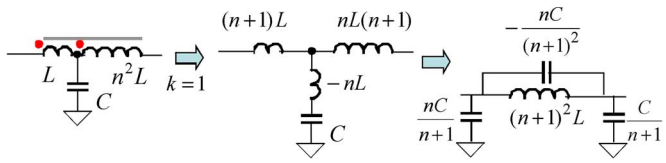

Fig. 7. Method 2: generation of negative capacitance to cancel the parasitic winding capacitance of an inductor with the help of direct coupling.

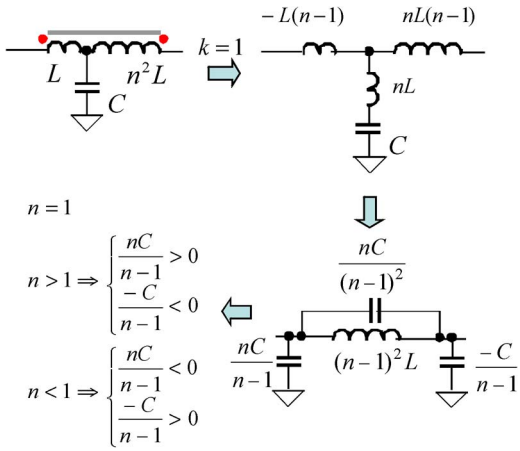

Fig. 8. Method 3: generation of negative capacitance on one side of the inductor to cancel parasitic capacitance with the help of inverse coupling.

B. Parasitic Cancellation Using Mutual Inductance

1) Principles: Some methods have been introduced to cancel the parasitic capacitance [2]–[6]. This section systematically investigates these methods and identifies the critical parameters for their performance. The negative capacitance can be equivalently generated using a small capacitor with the help of two coupled inductors. Depending on the connections and coupling polarities of these three components, there are four more methods that can be used to achieve this. Fig. 7 shows method 2.

In Fig. 7, two inductors with inductances L and n^2L are directly coupled on one core, where n is the turn ratio between the two inductors, and n^2 is the inductance ratio of the two inductors. A grounded capacitor C is connected to the inductors. If the coupling coefficient k is 1, with the help of Y-Δ network transformation, a π network can be derived. A negative capacitance is generated in parallel with inductors in the π network. This negative capacitance can cancel the winding capacitance since it is in parallel with the inductors. There are also two grounded positive capacitances generated on both sides. The values of these capacitances are shown in the figure.

On the other hand, if the two inductors in Fig. 7 are inversely coupled, the negative capacitance shows up on one side of the inductors in the π network. This situation is shown in Fig. 8. The values of all capacitances are shown in the figure.

In Fig. 8, the negative capacitance always shows up on the side of the inductor with the greater number of turns. The turn ratio n cannot be unity since it would null the total inductance. It is shown below that high n is good for parasitic capacitance cancellation. In power electronics circuits, power inductors are

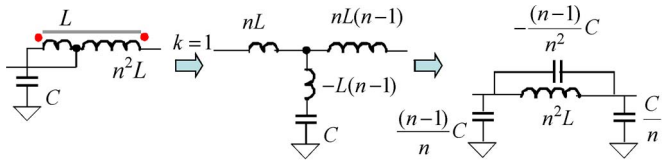

Fig. 9. Method 4: generation of negative capacitance to cancel parasitic winding capacitance of an inductor with the help of inverse coupling.

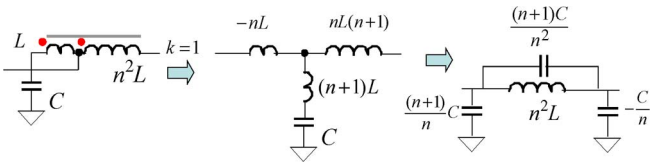

Fig. 10. Method 5: generation of negative capacitance on one side of the inductor to cancel parasitic capacitance with the help of direct coupling.

usually connected to power devices whose parasitic capacitance to a heat sink is the major source of CM noise due to the high dv/dt on power devices [4]. The cancellation method in Fig. 8 can be used to cancel the parasitic capacitance between the power devices and the heat sink, since the negative capacitance is on one side of the inductors. The generated negative capacitance is effectively parallel with the parasitic capacitance; therefore the total effect is cancellation if the two capacitances are equal. This method is referred to as method 3.

Rearranging the two coupled inductors and the grounded capacitor, methods 4 and 5 are derived to generate a negative capacitance, as shown in Figs. 9 and 10.

In Fig. 9, two inductors are inversely coupled and the cancellation capacitance is grounded on one side. The input/output port is connected to the other side or to the tap of the two inductors. If turn ratio n is larger than 1, a negative capacitance is generated in parallel with the inductors in the π network in Fig. 9. This method can be used for the cancellation of the inductors' winding parasitic capacitance if the negative capacitance is equal to the winding parasitic capacitance. Two grounded positive capacitances are generated on each side, and their values are shown in Fig. 9.

In contrast to Fig. 9, two inductors are directly coupled in Fig. 10. As a result, the grounded negative capacitance is generated on one side of two inductors in the π network. Since the negative capacitance is on one side, the method can be used for the cancellation of parasitic capacitance between the power devices and the heat sinks. The cancellation effect is similar to the method in Fig. 8. There are other two positive capacitances generated, and their values are shown in the figure.

The advantage of methods 2 and 4 is that they can be applied to either DM or CM inductors. Sometimes, these methods can even be applied to both CM and DM inductors at the same time, which is discussed below. Another advantage of methods 2 and 5 is that the turn ratio can be one. Thus, using two windings and a bifilar winding structure, it is easy to achieve high couplings for best performance [3]. On the other hand, other methods need a high turn ratio to compensate the effects of nonideal couplings. This is to be discussed later. In addition, method 2 does not need an extra winding to achieve cancellation since both windings are part of the main inductor.

2) Effectiveness of Cancellation: In the analysis in Figs. 7–10, it is assumed that two inductors have a coupling coefficient k equal to 1. If the coupling is nonideal, the cancellation would not be good at HFs. For methods 2 and 4, analysis shows that the leakage inductance of the two inductors would resonate with cancellation capacitance C at HFs, which makes cancellation bad. For methods 2 and 4, the resonant frequency is given by (4) and (5), respectively. Equation (4) can be further simplified as (6) when n is much larger than one. Equation (5) can be further expressed as in (7). In (6) and (7), L_B is the inductance of the resultant inductor, and C_P is the parasitic capacitance to be canceled. These equations show that the higher the coupling coefficient or the turn ratio is, the wider the frequency range will be for the cancellation.

For methods 3 and 5, a nonideal coupling would lead to an equivalent negative inductance in series with the negative capacitance. The impedance of the negative inductance will be higher than the impedance of negative capacitance at HFs; as a result, the cancellation would not be good at HFs. The corner frequencies of good cancellations for methods 3 and 5 are given by (8) and (9). Equation (8) can be further simplified as (10) if turn ratio n is much larger than one. Equation (9) can be further expressed as (11). In (10) and (11), L_B is the inductance of the resultant inductor, C_{CM} is the parasitic capacitance to be canceled, and n is the turn ratio of two inductors. Equations (10) and (11) show that the higher the coupling coefficient or the turn ratio is, the wider the frequency range will be for the cancellation. This condition is therefore true for all four of these methods. We have

$$\omega_{C1} = \frac{1}{\sqrt{\frac{(1-k^2)n^2}{n^2+2kn+1}LC}} \tag{4}$$

$$\omega_{C2} = \frac{1}{\sqrt{(1-k^2)LC}} \tag{5}$$

$$\omega_{C1} \approx \frac{\sqrt{n}}{\sqrt{L_B C_P (1-k^2)}} \tag{6}$$

$$\omega_{C2} = \frac{\sqrt{n-1}}{\sqrt{L_B C_P (1-k^2)}} \tag{7}$$

$$\omega_{C3} = \frac{1}{\sqrt{\frac{(1-k^2)n^2}{n^2-2kn+1}LC}} \tag{8}$$

$$\omega_{C4} = \frac{1}{\sqrt{(1-k^2)LC}} \tag{9}$$

$$\omega_{C3} \approx \frac{\sqrt{n-1}}{\sqrt{L_B C_{CM} (1-k^2)}} \tag{10}$$

$$\omega_{C4} = \frac{\sqrt{n}}{\sqrt{L_B C_{CM} (1-k^2)}}. \tag{11}$$

For the same reason the parasitic capacitance is canceled using mutual capacitance, methods 2 and 4 are good for the parasitic capacitance with first-order approximation only.

The third constraint for methods 2–5 is that the cancellation capacitance is always larger than the parasitic capacitance to

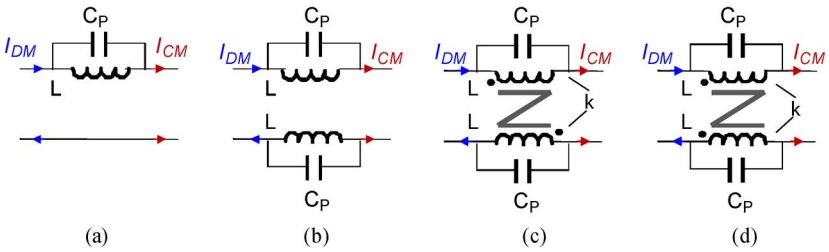

Fig. 11. Different inductor structures. (a) Single inductor. (b) Separate inductors. (c) Coupled DM inductor. (d) Coupled CM inductor.

be canceled. For CM applications, this may introduce more leakage current to the ground, and therefore, designers should pay attention to the capacitance value to be used.

One of the windings used in methods 3, 4, and 5 is the extra winding used to achieve cancellation. This additional winding may increase the size of the inductor, depending on the number of turns of the extra winding.

Because parasitic capacitance cancellation techniques can be used in either single-phase or multiphase power electronics circuits, it is obvious that the analysis in this paper can be applied to these applications.

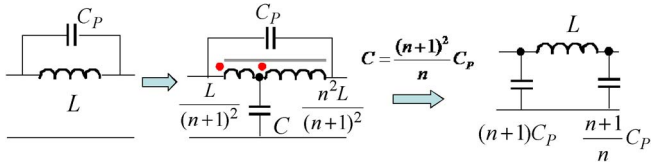

Fig. 12. Parasitic winding capacitance cancellation using method 2.

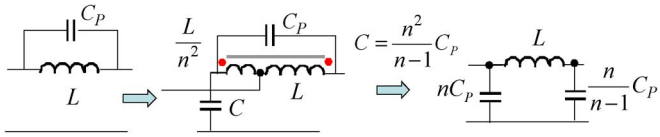

Fig. 13. Parasitic winding capacitance cancellation using method 4.

III. Applications of Parasitic Capacitance Cancellation

As discussed in Section II, cancellation techniques can be used to cancel the parasitic capacitance of an inductor or the parasitic capacitance between power devices and heat sinks. This section discusses methods for applying these techniques to different practical applications based on their characteristics.

A. Parasitic Capacitance Cancellation for Inductors

Conventionally, an inductor can be constructed in different ways, depending on function, the coupling polarities between two windings, and the connections to external circuits. Examples of this are shown in Fig. 11.

In Fig. 11(a), a single inductor is inserted to one power path, and its return path has no inductors. This is an unbalanced structure since the impedance on the two paths is different. This structure is usually used for DM noise suppression. Unless the CM impedance in the system is very high, the unbalanced impedance causes transformation between DM and CM noise [8]. In Fig. 11(b), two inductors are located separately on both power paths. Their inductances are the same. The structure is balanced so it does not cause any transformation between DM and CM noise, and the structure can suppress both DM and CM noise. For DM noise, the equivalent inductance is twice that of the single inductance. For CM noise, the equivalent inductance is half of the single inductance.

In Fig. 11(c), two inductors are directly coupled for DM noise and inversely coupled for CM noise. If the coupling coefficient k is unity, the DM inductance is four times the single inductance. The CM inductance is zero. Hence, this structure can only suppress DM noise. If the coupling coefficient k is smaller than unity, there is leakage inductance between the two inductors. The leakage inductance appears on both paths equally, but it is usually much smaller than coupled DM inductance. The effects of the leakage inductance on CM and DM noise for the structure in Fig. 11(c) can be analyzed similarly to that in Fig. 11(b).

In Fig. 11(d), two inductors are directly coupled for CM noise and inversely coupled for DM noise. If the coupling coefficient k is unity, the CM inductance is the same as the single inductance, and the DM inductance is zero. Hence, this structure can only suppress CM noise. If the coupling coefficient k is smaller than unity, there is leakage inductance between the two inductors. The leakage inductance appears on both paths equally, but is usually much smaller than the coupled CM inductance. The effects of the leakage inductance on CM and DM noise can be analyzed similarly to that in Fig. 11(b). In power electronics circuits, DM current is very high, and therefore, DM conductors are usually either inductors with low-permeability cores or the leakage of CM inductors. CM noise current is generated from the parasitic capacitance between the high dv/dt nodes and the ground, hence, its value is smaller than DM current. Because of this, the structures in Fig. 11(b) and (d) are usually used for CM inductors. On the other hand, the structures in Fig. 11(a)–(d) can all be used for DM inductors.

For each of the different functions and different inductor structures in Fig. 11, different parasitic capacitance cancellation techniques should be used. For the structure in Fig. 11(a), methods 2 and 4 can be used to cancel parasitic capacitance $C_{\rm P}$, as shown in Figs. 12 and 13. In Fig. 12, n is the turn ratio between two coupled windings. When n is equal to 1, the method used to cancel parasitic capacitance is the method proposed in [2] and [9]. In Fig. 13, the turn ratio cannot be unity; otherwise, the cancellation capacitance would be infinitely large. The cancellation in Fig. 12 is easier than that in Fig. 13 since a bifilar winding structure can be used to maximize the coupling

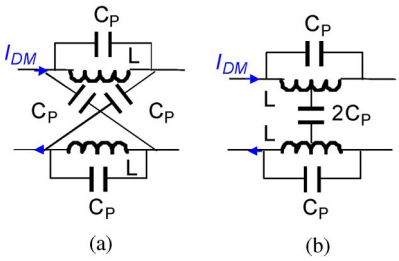

Fig. 14. DM C_P cancellation. (a) Using method 1. (b) Using method 2.

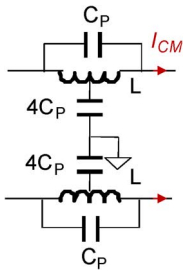

Fig. 15. CM C_P cancellation using method 2.

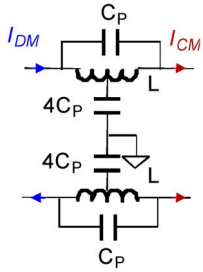

Fig. 16. DM/CM C_P cancellation using method 2.

coefficient when n is 1; hence, the cancellation can be achieved in a wider frequency range than that in Fig. 13.

For the structure in Fig. 11(b), since the two inductors can be either DM or CM inductors, the cancellation methods should be applied correspondingly. Because the two inductors are totally separate, the two inductors can be isolated, and the parasitic capacitance for CM and DM inductors are the same. When the two inductors are DM inductors, method 1, 2, or 4 can be used to cancel the parasitic capacitance. When the two inductors are CM inductors, method 2 or 4 can be used to cancel the parasitic capacitance. As mentioned above, it is easier to achieve good cancellation using method 2 than using method 4; thus, only methods 1 and 2 are discussed here. When the turn ratio is unity, the maximal coupling coefficient can be achieved for best cancellation via bifilar windings; hence, a unity turn ratio is preferred for method 2. Figs. 14 and 15 show how to apply the methods to cancel parasitic capacitance for DM and CM noise. Method 2 can be applied to both DM and CM at the same time, as shown in Fig. 16.

For the structure in Fig. 11(c), the CM inductance is the leakage inductance of the DM inductance; thus, it is very small. Only the cancellation for the DM parasitic capacitance is considered here. As discussed in [3], when two windings are on the same core, there are two kinds of parasitic capacitance. One is the parasitic capacitance within each winding. The other

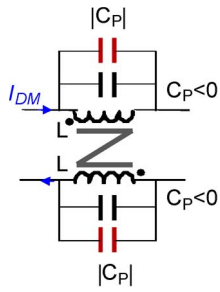

Fig. 17. C_P cancellation for a coupled DM inductor when C_P is negative.

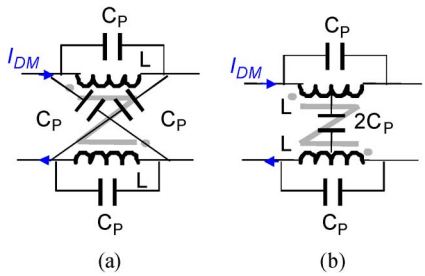

Fig. 18. C_P cancellation for a coupled DM inductor when C_P is positive. (a) Using method 1. (b) Using method 2.

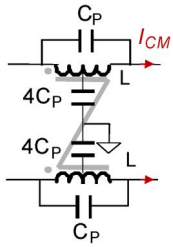

Fig. 19. C_P cancellation for a coupled CM inductor using method 2.

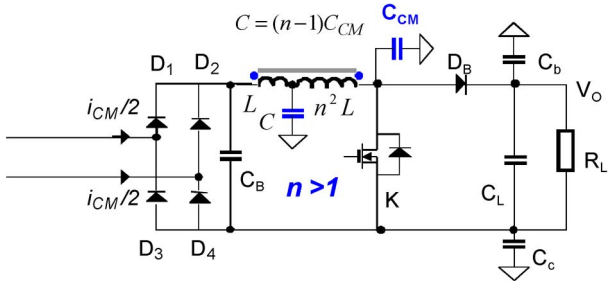

Fig. 20. Parasitic capacitance cancellation for a PFC converter using method 3.

is the parasitic capacitance between two windings. Based on network theory, the effects of the parasitic capacitance between two windings can be represented by paralleling a negative half-capacitance to each winding. Depending on the values of the two, the total capacitance C_P could be positive or negative. When C_P is negative, two small capacitors with a capacitance equal to $|C_P|$ can be paralleled to the windings to cancel C_P, as shown in Fig. 17. When C_P is positive, there are three ways to cancel it, i.e., using method 1, 2, or 4. Methods 1 and 2 are shown in Fig. 18.

In the structure in Fig. 11(d), since the CM inductance is much larger than its leakage, i.e., the DM inductance, only the

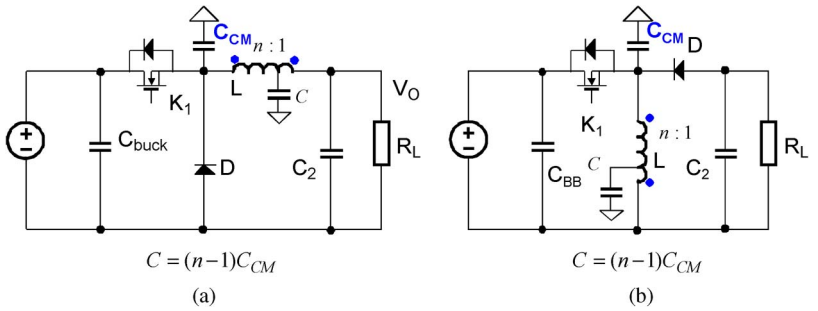

Fig. 21. Parasitic capacitance cancellation using method 3 for (a) a buck converter and (b) a buck–boost converter.

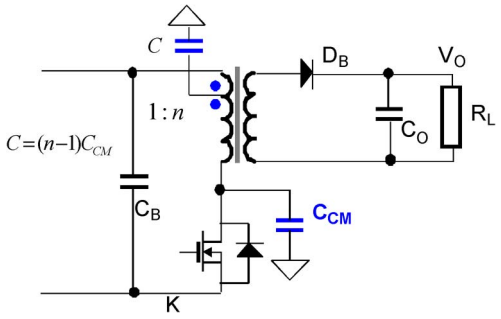

Fig. 22. Parasitic capacitance cancellation for a fly-back converter using method 3.

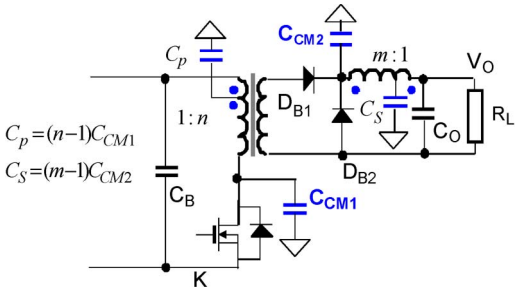

Fig. 23. Parasitic capacitance cancellation for a forward converter using method 3.

cancellation of CM $C_{\rm P}$ will be discussed here. Either method 2 or 4 can be applied to cancel parasitic capacitance. Method 2 is used here. The cancellation method is shown in Fig. 19.

B. Cancellation of the Parasitic Capacitance Between Power Devices and Heat Sinks

To cancel the parasitic capacitance between power devices and heat sinks, method 3 or 5 can be used. Based on (10) and (11), as the turn ratio goes up, the cancellation improves. Thus, the winding with a smaller number of turns should have only one turn. The two methods can achieve similar cancellation effects. Figs. 20–24 show some typical applications for method 3.

Fig. 20 shows the application of method 3 to a power-factor-corrected (PFC) converter, where the parasitic capacitance between the drain of a metal–oxide–semiconductor field-effect transistor (MOSFET) and the ground is canceled. When the heat sink is not grounded, cancellation capacitor C is connected to the heat sink only. In Figs. 21–24, the cancellation capacitor is connected to the heat sink, and the heat sink is grounded. If the heat sink is not grounded, the cancellation capacitor should still be connected to the heat sinks. In Figs. 23 and 24, both the parasitic capacitance between the drains of the MOSFETs and the heat sinks on the primary side and the parasitic capacitance between the cathode of the diodes and the heat sinks on the secondary side are canceled. In summary, the condition for cancellation is that one end of the coupled inductor is connected to a parasitic capacitance to be canceled, and the other end is connected to a node whose voltage potential is stable. The cancellation capacitor is connected to the tap of the two coupled inductors and to the heat sinks or other objects where the parasitic capacitance is concerned.

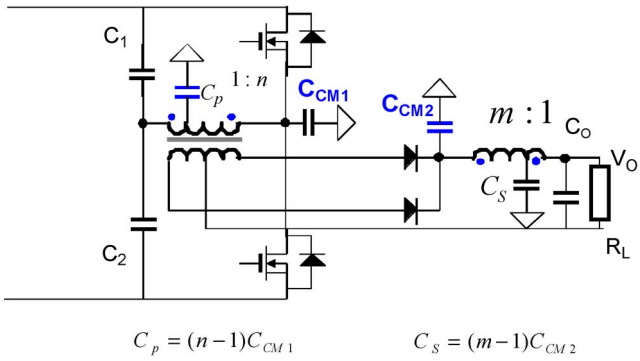

Fig. 24. Parasitic capacitance cancellation for a half-bridge converter using method 3.

It should be noted that in Figs. 23 and 24, if the secondary side is grounded or there are grounded CM capacitors connected to the secondary side, $C_{\rm CM2}$ does not cause CM noise on the primary side since the CM noise caused by $C_{\rm CM2}$ will go directly back to the secondary side. Thus, $C_{\rm CM2}$ may not need to be canceled for that case.

IV. Experimental Results

For the inductor structure with two inductors shown in Fig. 11(b), the experiments are carried out without DM parasitic capacitance cancellation and with DM parasitic capacitance cancellation. The cancellation method shown in Fig. 14(a) is used in the experiments. The cancellation condition described in (3) is met to cancel parasitic capacitance. The impedances of the two DM inductors are measured separately using an Agilent 4294A precision impedance analyzer. Based on an inductor's parallel *RLC* model [1], the inductance and $C_{\rm P}$ can be directly calculated via curve fitting. The 4294A analyzer has

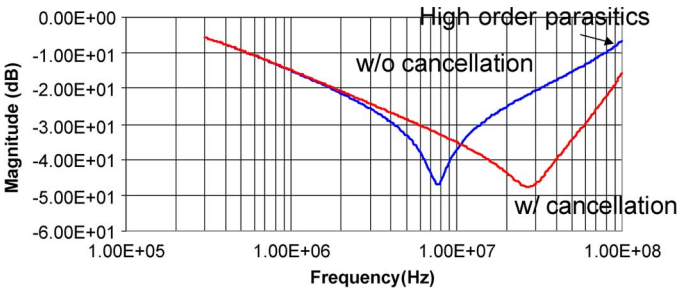

Fig. 25. Comparison of measured insertion gains before and after winding capacitance cancellation.

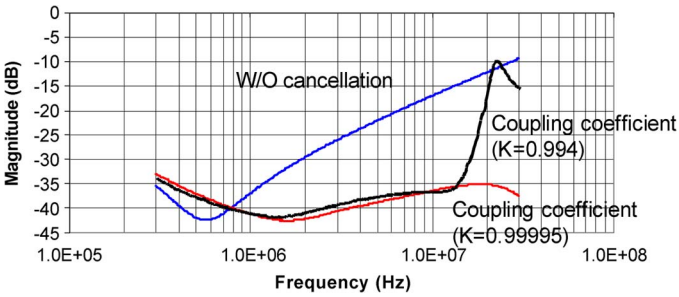

Fig. 26. Comparison of measured insertion gains before and after winding capacitance cancellation.

this function embedded, and therefore, it is easy to determine $C_{\rm P}$. The measured $C_{\rm P}$ for both inductors is around 10.7 pF.

An Agilent E5070B network analyzer is used to measure the insertion gains of the inductors. Fig. 25 shows the comparison between the measured insertion gains before and after the winding capacitance cancellation. The two cancellation capacitors are around 10 pF. After the cancellation, the inductor's resonant frequency, which is caused by the winding capacitance and inductance of the inductor, is increased from 8 to 28 MHz in Fig. 25. The inductor's filtering performance is improved from 10 MHz to beyond 100 MHz. At frequencies around 100 MHz, higher order parasitics begin to be dominant. As analyzed in Section II, the cancellation would no longer work efficiently.

For the inductor structure in Fig. 11(d), the implementation of the CM winding capacitance cancellation shown in Fig. 19 is applied with a turn ratio equal to one. $C_{\rm P}$ is calculated from the measured impedance using the same method used in the first experiment. It should be noted that for CM inductors, the impedance should be measured when two windings are in parallel. The $C_{\rm P}$ is around 9 pF, and the cancellation capacitance is 36 pF. Three measured insertion voltage gains are shown in Fig. 26. Compared with the case with lower coupling coefficient, the cancellation with higher coupling coefficient gives better performance above 12 MHz.

The cancellation for the parasitic capacitance C_{CM} between the MOSFET and the heat sink shown is applied to a boost PFC converter, as shown in Fig. 20. $C_{\rm CM}$ is measured using an Agilent 4294A analyzer. The device and heat sink are disconnected from the circuit before the capacitance measurement. The measured $C_{\rm CM}$ is 34.2 pF. The left winding has only one turn, hence, the largest turn ratio is achieved. This is good for the cancellation, as described in (10). The turn ratio is

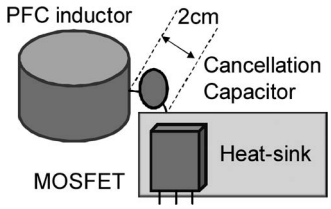

Fig. 27. Physical layout of a CM parasitic capacitance cancellation for a PFC converter using method 3.

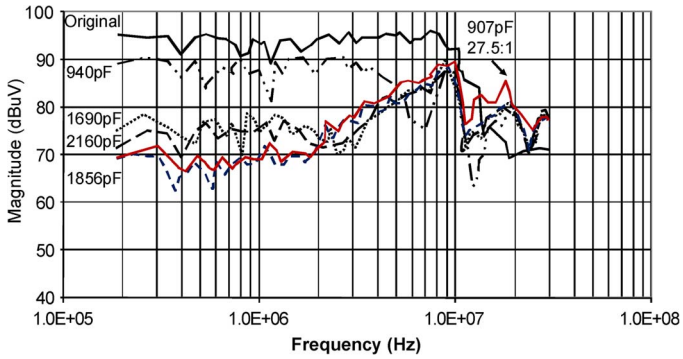

Fig. 28. Comparison of measured CM noise for a boost PFC before and after parasitic capacitance cancellation.

55 : 1, and therefore, the calculated cancellation capacitance is 1847 pF. In measurements, the cancellation capacitor changes from 940 to 2160 pF. The physical component layout and the comparison of the envelopes of the measured CM noise before and after cancellation are shown in Figs. 27 and 28. Experiments show that the best cancellation happens around 1856 pF, which is close to the calculated 1847 pF; 2160 pF is an overcancellation, which is not as good as 1856 pF. Because other noise sources exist in the PFC converter [10], the cancellation is not very sensitive to the cancellation capacitance around 1856 pF. For example, when the compensation capacitance varies from 1800 to 1900 pF, the measured CM noise varies by only several decibels. Fig. 28 shows that the low-frequency CM noise is greatly reduced. At HFs, due to the nonideal coupling of the two windings, the cancellation is not as good as it is at low frequencies. To demonstrate the effects of the turn ratio on the cancellation, the CM noise is also measured when the turn ratio of the inductor is 27.5 : 1. When the cancellation capacitance is 907 pF, which is close to the calculated cancellation capacitance of 920 pF, the lowest CM noise is measured. The measured noise is higher than the best case with 55 : 1 turn ratio above 10 MHz. This verifies the analysis in Section II.

The leakage current introduced by the cancellation capacitor is much smaller than the maximum leakage current of 3.5 mA that is allowed for this PFC converter. For a general case, the leakage currents of the whole system should be smaller than the limit specified by applicable safety standards.

By implementing several parasitic capacitance cancellation techniques in practical components and circuits, this section proves the previous analysis of these cancellation methods.

V. Conclusion

This paper has identified, studied, and generalized the advantages, constraints, critical parameters, and applications for

different parasitic capacitance cancellation techniques. It is found that all cancellation methods can only cancel the first-order parasitic capacitance. The working frequency ranges for the methods using mutual inductance are limited by the coupling between two windings. The higher the coupling coefficient is, the wider the cancellation frequency ranges will be. A high turn ratio between two coupled windings is good for cancellation at HFs.

Different cancellations have their own specific applications, which depend on the inductor structure. The method using the mutual capacitance concept is good for DM inductors with positive or negative winding capacitance, while the methods using the mutual inductance concept can cancel either the positive winding capacitance of an inductor or the parasitic capacitance between power devices and heat sinks. The experimental results agree with the theoretical analysis, which means that this analysis can help designers to select suitable cancellation techniques and to control critical parameters to get the best cancellation in their designs.

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